AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended): A testing device for a semiconductor integrated circuit which semiconductor integrated circuit incorporates a multiple number of D/A converters and outputs voltages from the D/A converters via associated output terminals, comprising:

a reference voltage generator which sequentially generates a multiple number of reference voltages, one reference voltage at a time, to be compared to each output voltage output from each of the output terminals and can selectively output multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits;

a multiple number of differential amplifiers, each having two input terminals, one for sequentially receiving the output voltage output from the associated output terminal and the other for sequentially receiving the reference voltage from the reference voltage generator; and

a comparator that receives the amplified output voltages from the multiple number of differential amplifiers and judges whether the amplified output voltage from each of the differential amplifiers falls within a given voltage range.

Claim 2 (original): The testing device for semiconductor integrated circuits according to Claim 1, wherein the reference voltage generator is a D/A converter which receives a digital data signal different from that of the D/A converters

incorporated in the semiconductor integrated circuit to generate the multiple number of reference voltages and can selectively output a necessary set of reference voltages from the multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits, in accordance with the selection of the digital data signal.

Claim 3 (currently amended): A testing method for a semiconductor integrated circuit, the semiconductor integrated circuit ~~which~~ incorporates a multiple number of D/A converters and outputs voltages from the D/A converters via associated output terminals, wherein a testing device for semiconductor integrated circuits is used which comprises:

a reference voltage generator which sequentially generates a multiple number of reference voltages, one reference voltage at a time, to be compared to each output voltage output from each of the output terminals and can selectively output multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits;

a multiple number of differential amplifiers, each having two input terminals, one for sequentially receiving the output voltage output from the associated output terminal and the other for sequentially receiving the reference voltage from the reference voltage generator; and

a comparator that receives the amplified output voltages from the multiple number of differential amplifiers and judges whether the amplified output voltage

from each of the differential amplifiers falls within a given voltage range, wherein the reference voltage generator includes a D/A converter which receives a digital data signal different from the signals to the D/A converters incorporated in the semiconductor integrated circuit to generate the multiple number of reference voltages and can selectively output a necessary set of reference voltages from the multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits, in accordance with the selection of the digital data signal, the method comprising:

the first step for calculating the difference between the reference voltage generated from the reference voltage generator of the testing device and the output voltage output from each output terminal, for all the output terminals;

the second step for amplifying the values obtained from the first step; and

the third step for judging at one time whether all the amplified differential values obtained in the second step in association with respective output terminals fall within the first given voltage range.

Claim 4 (original): The testing method for semiconductor integrated circuits according to Claim 3 comprising the above first through third steps, wherein even if the output from the device under test varies, the first given voltage range can be kept at constant by computing the difference between the output from the device under test and the associated reference voltage generated from the above reference voltage.

Claim 5 (original): The testing method for semiconductor integrated circuits according to Claim 3, further comprising:

the fourth step for decreasing the width of the first given voltage range by a multiple of the predetermined voltage width to set up a second given voltage range; and

the fifth step for judging at one time whether all the amplified differential values associated to respective output terminals fall within the second given voltage range, wherein the fourth and fifth steps are repeated until the judgment at the fifth step changes.

Claim 6 (original): The testing method for semiconductor integrated circuits according to Claim 5, wherein, based on the value of the second given voltage range when the judgment at the fifth step changes, the devices under test are classified into a plurality of ranks.

Claim 7 (original): The testing method for semiconductor integrated circuits according to Claim 5, wherein the width of the second given range is made narrower as the above fourth and fifth steps are repeated.

Claim 8 (currently amended): A storage medium for storing the program for a computer to execute a testing method for ~~a~~ semiconductor integrated circuits,

each semiconductor integrated circuit ~~which~~ incorporates a multiple number of D/A converters and outputs voltages from the D/A converters via associated output terminals, wherein a testing device for semiconductor integrated circuits is used which comprises:

a reference voltage generator which sequentially generates a multiple number of reference voltages, one reference voltage at a time, to be compared to each output voltage output from each of the output terminals and can selectively output multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits:

a multiple number of differential amplifiers, each having two input terminals, one for sequentially receiving the output voltage output from the associated output terminal and the other for sequentially receiving the reference voltage from the reference voltage generator; and

a comparator that receives the amplified output voltages from the multiple number of differential amplifiers and judges whether the amplified output voltage from each of the differential amplifiers falls within a given voltage range, wherein the reference voltage generator includes a D/A converter which receives a digital data signal different from the signals to the D/A converters incorporated in the semiconductor integrated circuit to generate the multiple number of reference voltages and can selectively output a necessary set of reference voltages from the multiple sets of reference voltages required for testing multiple kinds of

semiconductor integrated circuit, in accordance with the selection of the digital data signal, the program comprising:

the first step for calculating the difference between the reference voltage sequentially generated from the reference voltage generator of the testing device and the output voltage sequentially output from each output terminal, for all the output terminals;

the second step for amplifying the values obtained from the first step; and

the third step for judging at one time whether all the amplified differential values obtained in the second step in association with respective output terminals fall within the first given voltage range, wherein even if the output from the device under test varies, the first given voltage range can be kept at constant by computing the difference between the output from the device under test and the associated reference voltage generated from the above reference voltage.

Claim 9 (previously amended): A storage medium for storing the program for a computer to execute a testing method for a semiconductor integrated circuits which incorporates a multiple number of D/A converters and outputs voltages from the D/A converters via associated output terminals, wherein a testing device for semiconductor integrated circuits is used which comprises:

a reference voltage generator which generates a multiple number of reference voltages to be compared to each output voltage output from each of the

output terminals and can selectively output multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits:

a multiple number of differential amplifiers, each having two input terminals, one for receiving the output voltage output from the associated output terminal and the other for receiving the reference voltage from the reference voltage generator: and

a comparator that receives the amplified output voltages from the multiple number of differential amplifiers and judges whether the amplified output voltage from each of the differential amplifiers falls within a given voltage range, wherein the reference voltage generator includes a D/A converter which receives a digital data signal different from the signals to the D/A converters incorporated in the semiconductor integrated circuit to generate the multiple number of reference voltages and can selectively output a necessary set of reference voltages from the multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuit, in accordance with the selection of the digital data signal, the program comprising:

the first step for calculating the difference between the reference voltage generated from the reference voltage generator of the testing device and the output voltage output from each output terminal, for all the output terminals; the second step for amplifying the values obtained from the first step;

the third step for judging at one time whether all the amplified differential values obtained in the second step in association with respective output terminals

fall within the first given voltage range, wherein even if the output from the device under test varies, the first given voltage range can be kept at constant by computing the difference between the output from the device under test and the associated reference voltage generated from the above reference voltage;

the fourth step for decreasing the width of the first given voltage range by a multiple of the predetermined voltage width to set up a second given voltage range: and

the fifth step for judging at one time whether all the amplified differential values associated to respective output terminals falls within the second given voltage range, wherein the fourth and fifth steps are repeated until the judgment at the fifth step changes.

Claim 10 (original): The storage medium for storing the program for a computer to execute the testing method for semiconductor integrated circuits according to Claim 9, wherein, based on the value of the second given voltage range when the judgment at the fifth step changes, the devices under test are classified into a plurality of ranks.

Claim 11 (original): The storage medium for storing the program for a computer to execute the testing method for semiconductor integrated circuits according to Claim 9, wherein the width of the second given range is made narrower as the above fourth and fifth steps are repeated.